Noise Mitigation Capability Comparison: Power Bus Isolation vs. Power Plane Segmentation

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Abstract

In the printed circuit board design it usually implements two methods to solve the power-bus noise interference problem. One is by adding decoupling capacitor and the other method is to adopt power bus isolation or power plane segmentation. Large isolation gap distance gets better isolation impedance and it consequently improves the high frequency power-bus noise elimination capability. Meanwhile another important factor needed to consider is the segmentation pattern, the implementation cost will determine the segmentation size of the isolation area. Unavoidable interference exists in the digital and analog circuits that using the common power source. In this paper we will search and discuss several commonly implemented isolation techniques and study how to reduce the interference effect. By using isolated power island will apparently reduce board's impedance and the location of the power island will affect the board's resonant structure. The bridge width of the connecting bridge appreciably affects on the first resonant location, the segmentation gap size affects the coupling amount. The larger the gap size the smaller the gap capacitance will be and consequently larger gap size will improve the noise isolation capability; different gap shapes will affect the board's resonant structure, better board's resonant structure will improve resonant probabilities and consequently increase the board impedance.

***Key Words*:** Power Bus Noise, Decoupling Capacitor, Power Isolation Island

1. Introduction

In recent years the operating frequency in the integrated circuit is ever constantly increasing due to the advancement of the integrated circuit fabrication techniques. The signal rising and falling interval become shorter and the transition speed between high and low voltages becomes fast that it incurs the signal integrity problem that in signal transmission it will suffer reflection and crosstalk effects. This signal integrity issue is not only happening in the transmission line but it is also appearing in the bond wire between the die and the package, in the passage between PCB boards, and also in the connector connecting two boards [1]. In addition, radiation effect is possibly induced when a very high frequency signal is transmitting through a short transmission line, it is possibly inside the board to generate interference between signal wires, while some of the signals will radiate to the outside of the board through the connecting port, the so called Electromagnetic interference (EMI) effect.

The circuit size becomes smaller with IC fabrication technologies, and the thickness of the oxide layer has accordingly been reduced. It needs to lower the IC supply voltage to prevent the surging of the voltage through the oxide layer. While lower the supply voltage, it needs relatively to increase the current so as to provide sufficient

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power to drive the IC, it then requires to lowering the impedance between PCB boards to prevent too much power consumption in its transmission from generating an insufficient supply voltage. It becomes a critical issue of knowing how to reduce the impedance in the PCB power plane so as to maintain the power integrity. A conventional method to provide normal supply voltage for high frequency and high speed PCB board is by adding decoupling capacitor between the power plane and the ground plane [2,3].

From frequency domain point of view, it can use capacitor to lower the impedance in the PCB board so as to minimize the current power consumption to its possible extent; while from time domain consideration, it can use capacitor to provide instant current to IC and maintain its normal operation. However it has been observed that [4], in high operating frequencies, the decoupling capacitor will be unable to effectively reduce the impedance or provide sufficient instant current, second method is considered and followed. It considers to change the structure of the PCB power plane such as the use of PCB material with high permeability constant (ε_r) or use thinner dielectric material. Either measure will enable to effectively reduce the high frequency band impedance in the PCB board but its cost will also be increased. In this paper we will investigate the possibility of using least expensive material FR4, and by implementing segmentation and isolation measures to change the structure of the power plane so as to effectively mitigate the high frequency noise interference and to maintain the power integrity by effectively reducing the impedance. The effects of gap size of the isolated power island, the width of the connecting bridge, the plane gap size and the gap shape etc. are the tasks will be fully investigated in this paper [5,6].

2. Effect with Isolated Power Island

The theoretical calculation to find out the power impedance is by using Leis' proposed formula [7].

$$Z_{ij} = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left(\frac{j\omega\mu h C_m^2 C_n^2}{P_x P_y (k_{xm}^2 + k_{yn}^2 - k^2)}\right)\cos(k_{xm}T_{xi}) \times \cos(k_{xm}T_{xj}) \times \cos(k_{yn}T_{yi}) \times \cos(k_{yn}T_{yj}) \times \operatorname{sinc}\left(\frac{k_{xm}L_{xi}}{2}\right) \times \operatorname{sinc}\left(\frac{k_{xm}L_{xj}}{2}\right) \times \operatorname{sinc}\left(\frac{k_{yn}L_{yi}}{2}\right) \times \operatorname{sinc}\left(\frac{k_{yn}L_{yj}}{2}\right)$$

where Px and Py represent the printed circuit boards widths in the x- and y-directions, respectively, h is the height of the printed circuit boards, Txi, Txj, Tyi and Tyj are the coordinates of the center of the ith and jth ports in the x- and y-directions, respectively, Lxi, Lxj, Lyi and Lyj are much less than the wavelengths of interest and represent the ith and jth port widths in the x- and y-directions, respectively, k represents the real wavenumber for the lossless case, $k = \omega\sqrt{\mu\varepsilon}$, $k_{xm} = \left(m\pi / P_x\right)$, and $k_{yn} = \left(n\pi / P_y\right)$. The first one is a constant factor, $\frac{\mu d C_m^2 C_n^2}{P_x P_y}$, the second one Green's function factor, $\frac{j\omega}{k_{xm}^2 + k_{yn}^2 - k^2}$, is the only one dependent on frequency, defines the locations of the poles and peaks in the system impedance. The third one is cosine factor which decides the variation of the impedance value when the circuit printed boards are in different positions. In different coordinate, the impedance value will be different. The fourth one is sinc factor which is related to the segmentation of the PCB. Through this formula, we can find out the resonant frequency and can also discuss the affect of position on impedance. When the size of the printed circuit boards becomes bigger, lower the resonant frequency is and closer to the center it is, because of cosine, some resonant points can be eliminated.

It is known that the resonance does not often occur in the central region from the slab waveguide calculation. Thus, the board impedance in the central region is usually lower than that in other region. It is why many main chips or noisy chips are placed at the central region of the PCB board because it will have more capability to suppress noise and result in less noise to interfere other components in PCB board. It is noted that the resonance in the different size of the power island occurs at different frequency. A small size of the power island has higher resonant frequency. For the resonance mitigation of the power island, two parameters of bridge width and gap separation have significantly important effects. The small bridge width and large gap separation will effectively suppress noise migration to other region.

If we know in the circuit board, an IC or an area is the source of generating noise interference, we can try to use

isolated power island to mitigate this interference effect. A power-plane test board with isolate power island is shown in Figure 1. The test board material is made of FR4, it is a double-side board, and the board size is 15 cm × 9 cm with board thickness of 0.8 mm. It uses segmentation to isolate a rectangular area in the lower left corner and uses only a conducting bridge to conduct and connect both areas. In the set up, the power plane is configured in the upper plane while the lower plane is the reference ground plane. Two ports are located at (30 mm, 25 mm) and (120 mm, 65 mm) respectively. A HP8753D vector network analyzer is used to measure the S parameter characteristics and then uses approximate formulas (1) and (2) [8] to translate the measured S parameters into a relationship of impedance vs. frequency.

$$S_{21} = \frac{Z_{21}}{Z_{21} + \frac{1}{2}Z_O} \tag{1}$$

where Z_{21} is the printed circuit board transfer impedance form port 1 to port 2, and $Z_o = 50$ ohms is the characteristic impedance of the measurement system. For $Z_{21} << Z_o$, which is generally the case, except possibly at the parallel-resonance frequencies,

$$|S_{21}| \approx \frac{|Z_{21}|}{25} = (|Z_{21}| - 28)\ \text{dB} \tag{2}$$

The lower the $|S_{21}|$ is, the better the isolation is.

In Figure 2, the black line is the board with continuous plane without using power island while A, B, C are three different boards implemented with power islands. The red line one has size d = 2.5 mm and s = 2.5 mm while for the green line one it has size d = 5 mm and s = 2.5 mm, and it is d = 2.5 mm and s = 5 mm for the black line board. From the plot it is obviously that each of the three boards with power island structure has overall impedance much lower than the board without using power island structure. This is because the board with power island structure is not perfect with some destruction comparing with the board without using power island structure so that it has less resonant effect and consequently it has less impedance. By taking board A as reference, it has less inductance around 600 MHz for board B, this is because a wider conducting bridge is used in board B and consequently its noise mitigation effect is not as effective as board A. It has no significant difference in other two frequency bands. For board C, it has wider conducting bridge and comparatively it has larger impedance than that of board A in some frequency ranges but overall it has no significant difference between board A and board C that is implemented with incompletely isolated power island.

The isolated power island is located at Loc#1 and Loc#2 respectively for boards D and E, as shown in Figure 3. Figure 4 shows the comparing performance of continuous plane board with boards D and E that are implemented with completely isolated power island. In Figure 4, it appears that the noise interference in the boards with completely isolated power island is reducing by 20–30 dB comparing with continuous plane board. Comparing boards D and E, the resonant effect in board

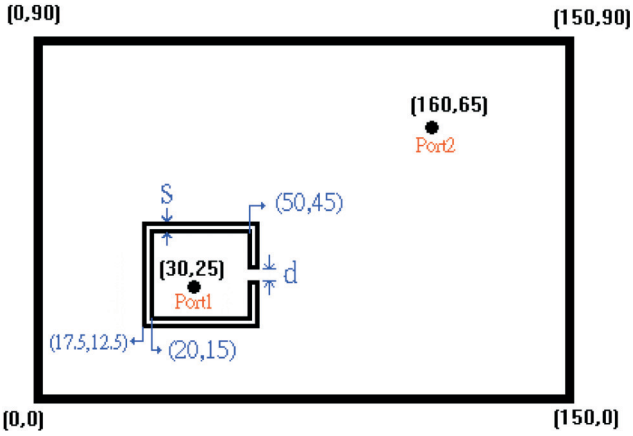

Figure 1. The power plane test board with isolated power island.

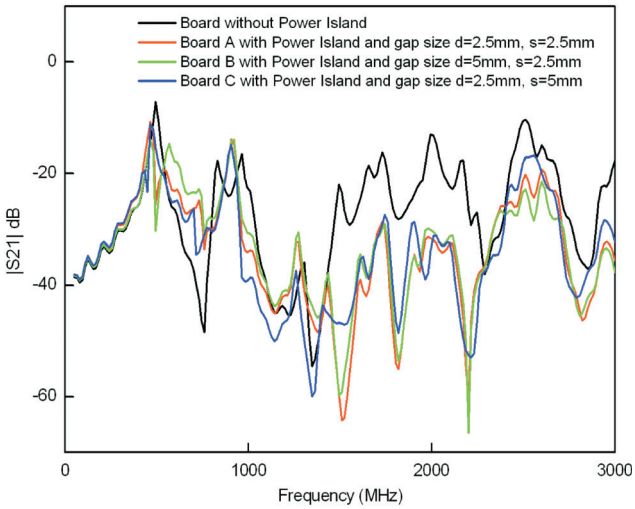

Figure 2. S21 with different gap size of isolated power island.

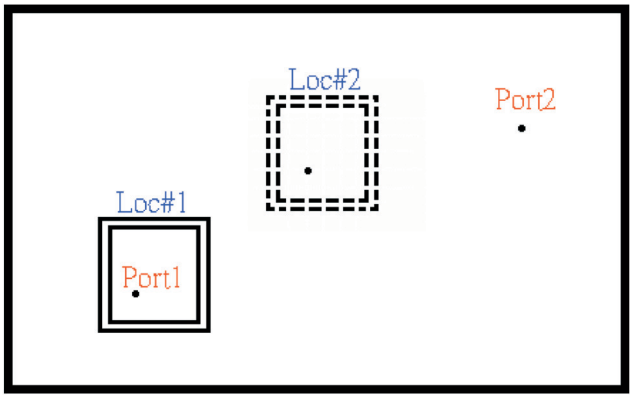

Figure 3. The board with different placement locations of isolated power islands.

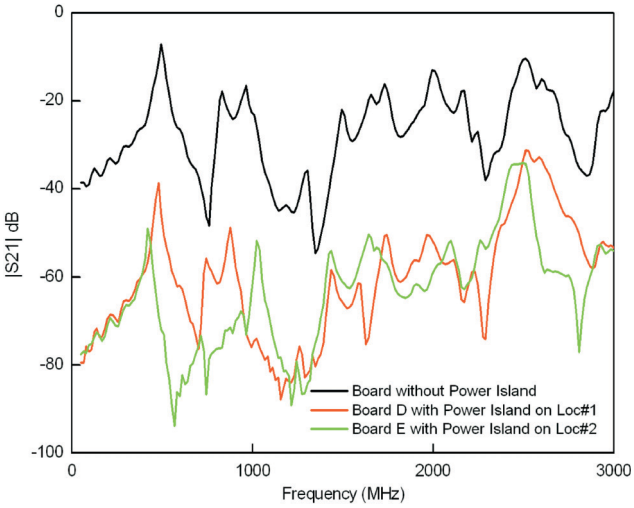

Figure 4. S21 with different placement locations of isolated power islands.

E is reduced a lot comparing with that of board D. This is because when the wave propagates through the board it has smaller peak amplitude around the central location and consequently its resonant effect at the central location is smaller than at other locations. Consequently, different placement locations of power islands will introduce different effects on the power supply system.

3. Bridges Interconnection

We consider the situation of two circuits interfering with each other but they share the same power sources, for example in a circuit board it consists of digital and analog circuits. In digital circuit it has only voltage transitions between high and low bits, when the operating frequency is high the voltage transition speed between voltage levels becomes fast and such high speed voltage transition will induce ground bound noise. Furthermore when many digital signals happen to make transitions simultaneously it will generate SSN (simultaneous switching noise) effect. Therefore we know that it is quite easy to generate noise signal in digital circuit, on the other hand in the analog circuit the noise interference has great effect on the circuit performance. The resulting Signal to Noise Ratio (SNR) in the analog circuit is low comparing with that in the digital circuit. Therefore the analog signal is more easily to suffering noise interference when common power planes are interconnected together in the analog and digital circuits. The bridge interconnection as shown in Figure 5 can be used to reduce this kind of noise interference.

The width of the thin wire interconnecting two areas will also affect the whole board characteristics. We consider three different widths, 2 mm, 5 mm and 10 mm for the dimension, as shown in Figure 5. We then use a vector network analyzer to measure S parameters and then use approximate formulas to convert these S parameters into their corresponding impedance vs. frequency relationship as shown in Figure 6. The generation of the first resonant point can be considered as resulting from many thin wires that were used in the interconnections. When it uses narrow interconnecting wires it results in larger inductance and consequently lower resonant frequency is generated and vice versa, i.e. wide interconnecting wires will result in higher resonant frequency.

When the operating frequency is higher than 1 GHz, it appears that the S21 characteristics do not exhibit obvious differences in these three implementations with

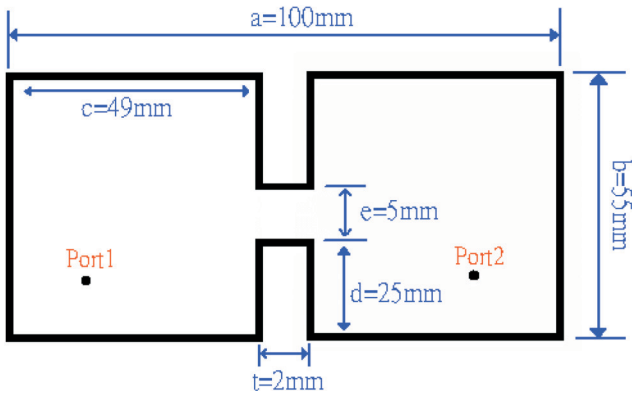

Figure 5. Test board with bridge interconnection.

different interconnecting wires widths. This is because the areas structures in both sides are not changed and their resonant locations are almost located at the same positions. If other parameters are fixed but the dimension c, as shown in Figure 5, is selected as 29 mm, 39 mm and 49 mm respectively then it has measurement results as shown in Figure 7 when a vector network analyzer is used. The line (c = 29 mm) one is obviously having lower second resonant location comparing with other two dimensions, this is because the area unbalance in the two sides of the board of the red line dimension has more influence than the effect resulting from the resonant location change. The locations of the higher resonant frequencies are also different when these three different c dimensions are implemented.

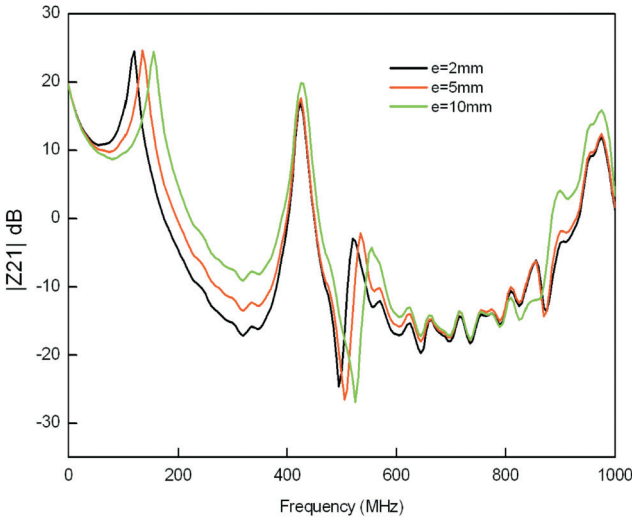

Figure 6. Z21s with e = 2 mm, 5 mm and 10 mm.

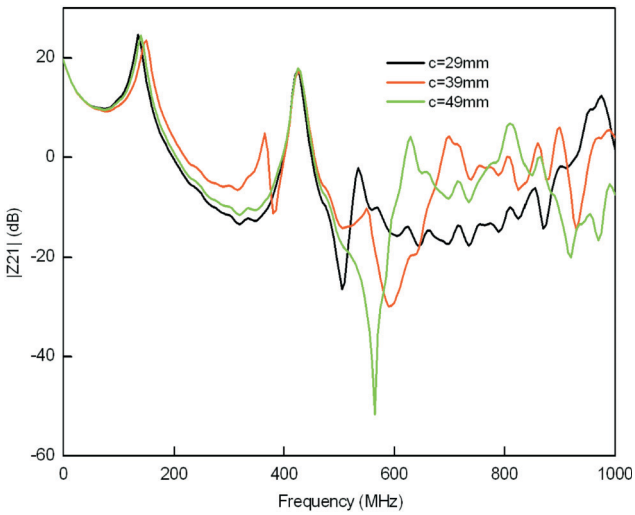

Figure 7. Z21s with c = 29 mm, 39 mm and 49 mm.

4. The Noise Mitigation Due to Different Plane Gap Sizes

In the mainframe design, it usually uses a large amount of ICs and components and consequently it needs to provide various levels of voltage sources. It sometimes in the design uses multilayer structure to place voltage sources in different layers. Multilayer structure can also be used to mitigate the noise signal, but its cost is high in the implementation. Another method to mitigate noise signal is to arrange by placing various voltage sources in the same board. In this fashion, the power plane will then be divided into many segments and the gap width between power segments will determine the noise interference effect between power segments.

We totally generate seven test boards and each board is a 6 in × 4 in rectangular dual plane that has the arrangement as shown in Figure 8, it cuts a straight line gap in the central part of the upper layer. The gap separation has sizes 16 mil, 32 mil, 64 mil, 125 mil, 250 mil, 500 mil and 1000 mil in each board, respectively. The test ports, port 1 and port 2 are located at the central positions of each board. It uses a vector network analyzer to measure the S parameter characteristics and then convert these measurements into the relation of impedance vs. frequency. Generally, this kind of power island structure is modeled as a π-network comprised of two shunt capacitors representing the inter-plane capacitances of the two islands and one series capacitor representing the coplanar gap capacitance [5]. As shown in Figure 9 is a lumped-element circuit model for the power island struc-

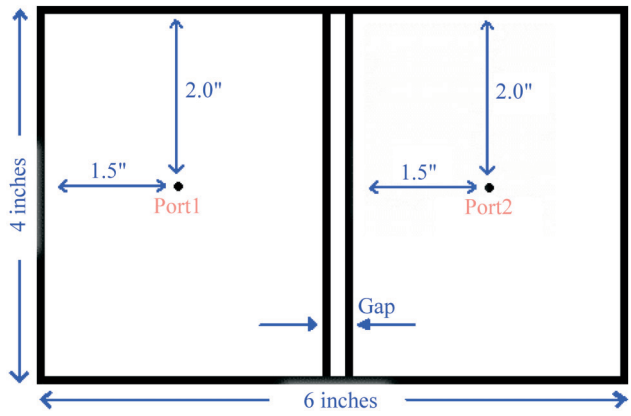

Figure 8. Test board with gap isolation in power plane.

ture. The larger the gap separation is, the smaller the gap capacitance and the higher the noise suppression are.

By observing Figure 10, it reveals that the shorter the gap size the larger the overall board impedance, and the noise generating from the current due to high impedance is also having high level that is not a favorable phenomena in the circuit design. It is also observed that when we increase the gap distance, the board impedance decreases accordingly; this phenomena can be explained from the concept of coupling amount. The relation of the gap between the two boards of the upper plane can be considered equivalently as a capacitor. When the gap size is short it has high capacitance and its resulting varactor impedance will be reduced and the probability of the noise signal passing through the gap becomes larger and vice versa. From Figure 10 it also appears that when the gap size is higher than 125mils, the decrease in the board impedance will not have an appreciable change.

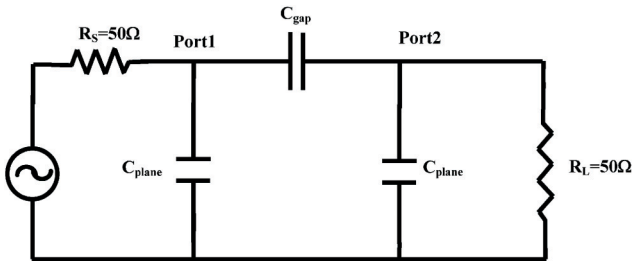

Figure 9. A lumped-element circuit model of the power island structure.

It needs to consider this observation and include it in the design and implementation of the circuit.

5. The Effect of Gap Shape on the Noise Mitigation

As mentioned in the previous paragraphs that different gap sizes in the power plane will result in different noise interference between voltage sources. Meanwhile the gap shape will also have effect on the noise interference. As shown in Figure 11 [6], three different gap shapes, straight line, triangle and rectangle are consi-

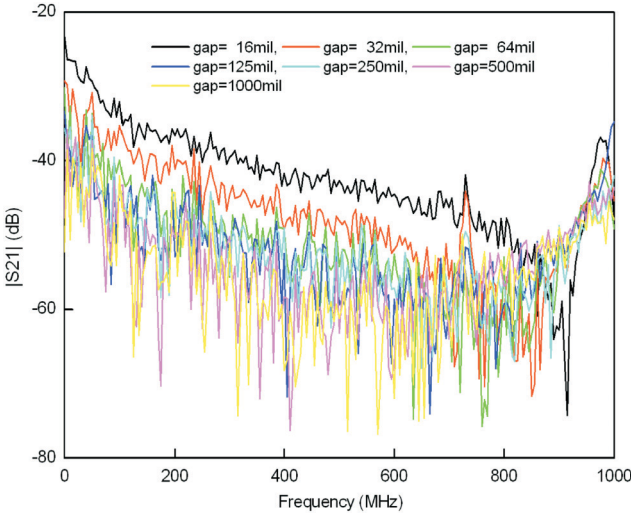

Figure 10. S21s from different gap sizes.

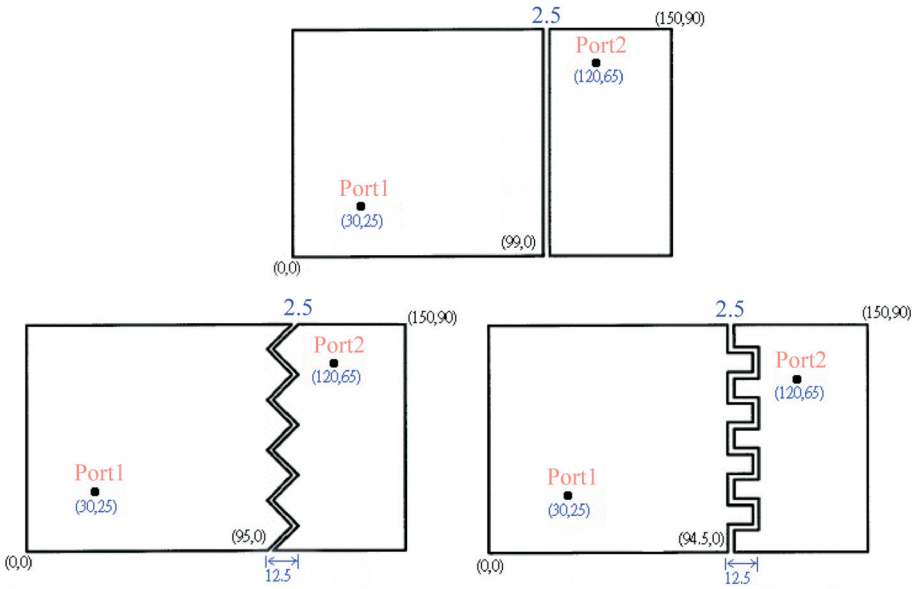

Figure 11. Test board with straight line, triangular and rectangular gap shapes.

dered. By using a vector network analyzer to measure their S parameters and converting them into a relation of impedance vs. frequency as shown in Figure 12. It shows that it has the largest impedance value with the straight line gap, and the triangular gap shape has the next largest impedance value. The rectangular gap shape has the best performance. The reasons for these results can be explained by combining the plots of S11, S21 and S22 parameters together and getting the results shown in Figures 13–15. When it incurs resonance in either S11 or S22, it also results resonance in S21. When it has resonance occurs simultaneously in S11 and S22, the resonant peak amplitude in S21 will be becoming larger. As we know the board with straight line gap will be less destructed than those with rectangular or triangular gap. When resonances happen on both sides of the gap then the probability these resonances have the same frequencies will be higher in the straight line gap than the other two gaps structures, and consequently it will have higher coupling amount and the overall board impedance will be higher. It is not easy to get conclusion just looking from the gap shape, which gap shape, rectangle or triangle, will be less destructive; but it can be concluded that the rectangular gap shape has less impedance value than that of the triangular gap shape. Different shapes of the power island will significantly affect the resonance mitigation capability. More regular shape (like straight line) has higher resonant peak due to con-

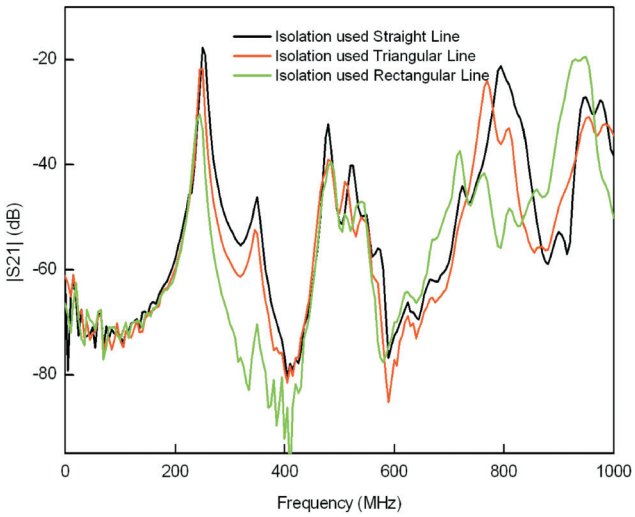

Figure 12. S21s of three different gap shapes.

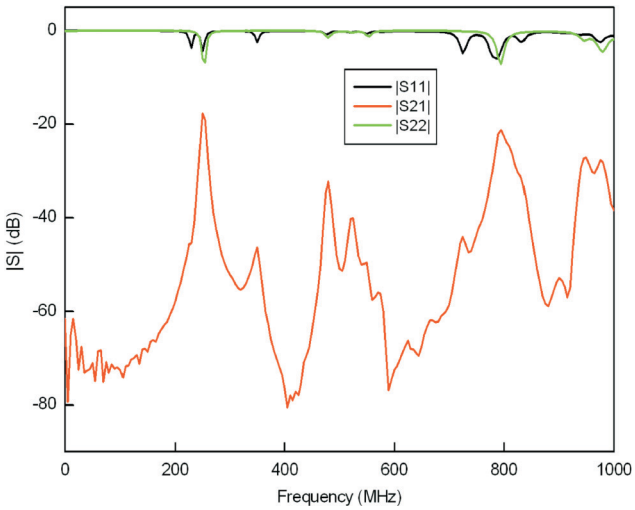

Figure 13. S11, S21, and S22 curves of straight line gap shape.

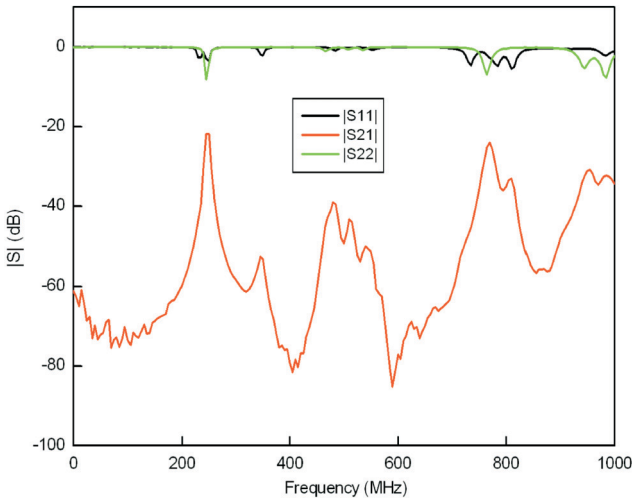

Figure 14. S11, S21, and S22 curves of triangular gap.

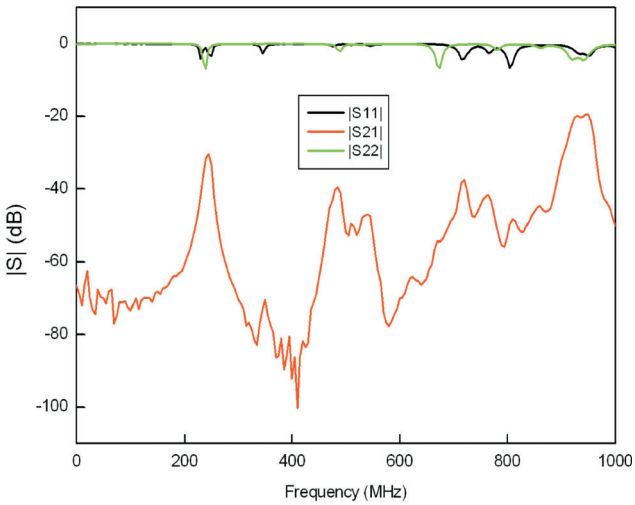

Figure 15. S11, S21, and S22 curves of rectangular gap.

structively resonant interference and results in poor resonant migration. Irregular shape has lower resonant peak due to destructively resonant interference and results in better resonant migration.

6. Conclusion

In this paper we demonstrated by utilizing the isolated power island technique to mitigate noise interference in the power plane. By comparing the final board impedance it revealed that it is about 5−10 dB lower in the isolated power island structure than the board without using any isolating island. When the board impedance is decreased the power consumption due to current flow will be reduced and then the voltage source will be less noise affected. It seems that the gap size of the conducting bridge for connecting power islands is not an important parameter in the noise mitigating operation it has only a small amount of difference in certain frequency ranges. Different power island locations will change board's resonant structure. Resonance is not easy to generate when the power island is located in the central area of the board, it concludes that the board impedance will be lower than other structures when the power island is located in the central part of the board.

In the interfering effect between analog and digital circuits, interference can be reduced by board segmentation, and varying the size of the conducting bridge will have only effect on the first resonant location. By changing the width of the segmentation area will alter the board structure and this board structure change has somewhat influence on the resonant effect.

It also concludes from the measurement data by varying the gap size that the gap capacitance is increased when smaller gap size is used. It knows from varactor impedance formula that larger capacitance value results in smaller varactor impedance that results in worse noise isolation. On the contrary larger gap size results in larger varactor impedance and consequently its capability of noise reduction becomes better. Different gap shapes also affect the noise mitigation capability. Three gap shapes such as straight line, triangular form or rectangular shape have been considered in the paper to analyze their resulting board impedances. It finds that the board is less destructed in the straight line gap shape it has higher probability to generate resonance that its board impedance is larger than other two gap shapes. On the other hand in the triangular or rectangular gap pattern the board has been destructed in more areas comparing with the straight line gap shape, it generates less resonant effect and consequently it has lower board impedance.

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